WHAT IS CLAIMED IS:

1. A fabrication method for a semiconductor device comprising the steps of:

(a) forming a gate electrode on a semiconductor region of a first conductivity type with a gate insulating film interposed therebetween;

(b) forming extension implanted layers in the semiconductor region by implanting first impurities of a second conductivity type in the semiconductor region using the gate electrode as a mask;

(c) after the step (b), forming fluorine implanted layers in the semiconductor region by implanting fluorine in the semiconductor region using the gate electrode as a mask; and

(d) after the step (c), forming extension diffused layers of the second conductivity type made from diffusion of the first impurities in top portions of the semiconductor region by performing first heat treatment.

2. The method of Claim 1, wherein the dose of fluorine in the step (c) is not less than $1 \times 10^{13}/cm^2$ and also in the level at which the semiconductor region is kept from becoming amorphous.

3. The method of Claim 1, wherein the dose of fluorine in the step (c) is less than $3 \times 10^{14}/cm^2$.

4. The method of Claim 1, wherein the implantation projected range of fluorine in the step (c) is roughly the same as the implantation projected range of the first impurities in the step (b).

5. The method of Claim 1, wherein the step (b) includes the step of forming pocket

implanted layers in the semiconductor region by implanting second impurities of the first conductivity type in the semiconductor region using the gate electrode as a mask, and

in the step (d), pocket diffused layers of the first conductivity type made from diffusion of the second impurities are formed in portions of the semiconductor region under the extension diffused layers by performing the first heat treatment.

6. The method of Claim 1, wherein after the step (d), the method further comprises the steps of:

(e) forming sidewalls made of an insulating film on walls of the gate electrode;

(f) forming source/drain implanted layers in the semiconductor region by implanting third impurities of the second conductivity type in the semiconductor region using the gate electrode and the sidewalls as a mask; and

(g) after the step (f), forming source/drain diffused layers of the second conductivity type made from diffusion of the third impurities in portions of the semiconductor region on the outer sides of the sidewall.

7. The method of Claim 1, wherein in the step (d), the fluorine in the fluorine implanted layers diffuses while interacting with point defects, so that excessive point defects induced in the semiconductor region are removed.

8. The method of Claim 1, further comprising the step of:

performing extremely low temperature heat treatment for the semiconductor region before the step (d) and after the step (c), to recover crystal damage produced in the semiconductor region due to the implantation of the first impurities and the fluorine without substantially allowing diffusion of the first impurities in the extension implanted

layers.

9. The method of Claim 8, wherein the extremely low temperature heat treatment has a heating temperature of 400° C to 600° C.

10. The method of Claim 1, wherein the first heat treatment in the step (d) is rapid thermal annealing in which the temperature rise rate is about 100° C/s or more, the temperature drop rate is about 80° C/s or more, the heating temperature is about 850° C to 1050° C, and the peak temperature is held for about ten seconds at the longest or is not held at all.

11. The method of Claim 1, wherein the first impurities in the step (b) are boron or indium.

12. The method of Claim 1, wherein the first impurities in the step (b) are arsenic.

13. The method of Claim 12, wherein during the first heat treatment in the step (d), the first impurities in the extension implanted layers diffuse in a state in which the fluorine has captured atomic vacancies produced in top portions of the semiconductor region.

14. The method of Claim 1, wherein the dose for the implantation of the first impurities in the step (b) is in a level at which the semiconductor region is kept from becoming amorphous, and

the extension diffused layers having a predetermined impurity concentration are formed by repeating a series of process steps composed of implanting the first impurities in

the step (b), implanting fluorine in the step (c) and performing the first heat treatment in the step (d).

15. A semiconductor device comprising:

a gate electrode formed on a semiconductor region of a first conductivity type with a gate insulating film interposed therebetween; and

extension diffused layers of a second conductivity type formed in portions of the semiconductor region on the sides of the gate electrode,

wherein the extension diffused layers are crystal layers that contain fluorine and are free from residual defects.